Claims

What is claimed is:

[c1] A method for optimizing decoupling capacitance in a delay locked loop, comprising:

inputting a representative power supply waveform having noise to a simulation of the delay locked loop;

estimating jitter of the delay locked loop;

adjusting an amount of decoupling capacitance; and

repeating the inputting, estimating, and adjusting until the jitter falls below a selected amount.

[c2] The method of claim 1, wherein the representative power supply waveform is obtained from a physical system.

[c3] The method of claim 2, wherein the physical system comprises a printed circuit board.

[c4] The method of claim 2, wherein the physical system comprises a chip package.

[c5] The method of claim 2, wherein the physical system comprises a chip.

[c6] The method of claim 1, wherein the representative power supply waveform is obtained from a location on a physical system adjacent to an intended location of the delay locked loop.

[c7] The method of claim 1, wherein the representative power supply waveform is obtained from a simulation of a power supply.

[c8] The method of claim 7, wherein the simulation of the power supply is performed using a first simulation tool and the simulation of the delay locked loop is performed using a second simulation tool.

[c9] The method of claim 1, wherein the representative power supply waveform comprises a noise waveform combined with a power supply waveform.

[c10] The method of claim 1, wherein the representative power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

[c11] The method of claim 1, wherein the simulation of the delay locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

[c12] A computer system for optimizing decoupling capacitance in a delay locked loop, comprising:

a processor;

a memory; and

software instructions stored in the memory adapted to cause the computer system to:

input a representative power supply waveform having noise to a simulation of the delay locked loop;

estimate jitter of the delay locked loop;

adjust an amount of decoupling capacitance; and

repeat the input, estimate, and adjust until the jitter falls below a selected amount.

[c13] The computer system of claim 12, wherein the representative power supply waveform is from a physical system.

[c14] The computer system of claim 13, wherein the physical system comprises a printed circuit board.

[c15] The computer system of claim 13, wherein the physical system comprises a chip package.

[c16] The computer system of claim 13, wherein the physical system comprises a chip.

[c17] The computer system of claim 12, wherein the representative power supply waveform is obtained from a location on a physical system adjacent to an intended location of the delay locked loop.

[c18] The computer system of claim 12, wherein the representative power supply waveform is obtained from a simulation of a power supply.

[c19] The computer system of claim 18, wherein the simulation of the power supply is performed using a first simulation tool and the simulation of the delay locked loop is performed using a second simulation tool.

[c20] The computer system of claim 12, wherein the representative power supply waveform comprises a noise waveform combined with a power supply waveform.

[c21] The computer system of claim 12, wherein the representative power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

[c22] The computer system of claim 12, wherein the simulation of the delay locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

[c23] A computer-readable medium having recorded thereon instructions executable by a processor, the instructions adapted to:

input a representative power supply waveform having noise into a simulation of a delay locked loop;

estimate jitter of the delay locked loop;

adjust an amount of decoupling capacitance; and

repeat the input, estimate, and adjust until the jitter falls below a selected amount.

[c24] The computer-readable medium of claim 23, wherein the representative power supply waveform is determined from a physical system.

[c25] The computer-readable medium of claim 24, wherein the physical system comprises a printed circuit board.

[c26] The computer-readable medium of claim 24, wherein the physical system comprises a chip package.

[c27] The computer-readable medium of claim 24, wherein the physical system comprises a chip.

[c28] The computer-readable medium of claim 23, wherein the representative power supply waveform is obtained from a location on a physical system adjacent to an intended location of the delay locked loop.

[c29] The computer-readable medium of claim 23, wherein the representative power supply waveform is obtained from a simulation of a power supply.

[c30] The computer-readable medium of claim 29, wherein the simulation of the power supply is performed using a first simulation tool and the simulation of the delay locked loop is performed using a second simulation tool.

[c31] The computer-readable medium of claim 23, wherein the representative power supply waveform comprises a noise waveform combined with a power supply waveform.

[c32] The computer-readable medium of claim 23, wherein the representative power supply waveform is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.

[c33] The computer-readable medium of claim 23, wherein the simulation of the delay locked loop is dependent on at least one selected from the group consisting of temperature, voltage, frequency, and manufacturing process.